Assignee: Intel Corporation

Dkt: 884.513US1 (INTEL)

REMARKS

This paper responds to the Office Action mailed on January 25, 2006.

Claims 9, 13, 14, 16, and 17 are amended. Claims 2-17 and 19-28 remain pending in this application.

§112 Rejection of the Claims

Claims 13, 16, and 17 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant respectfully traverses. Claim 13, 16, and 17 are amended for clarity. Applicant submits that claims 13, 16, and 17, as amended, particularly point out and distinctly claim the subject matter which applicant regards as the subject matter of the invention.

§102 Rejection of the Claims

Claims 9-12 and 17 were rejected under 35 USC § 102(b) as being anticipated by Leung et al. (U.S. 5,799,051, hereinafter Leung).

Applicant respectfully traverses for at least the reasons presented below.

Claim 9 is amended and recites, among other things, a phase detector and control circuit to compare a phase of a "data signal" and a phase of a "clock signal" on the output clock node and to create interpolator control signals, the "phase detector including a clock node to receive the clock signal from the input clock node, and a data node to receive the data signal".

Leung teaches in FIG. 2 a phase detector 128 to compare a phase of a clock signal RCLKs 42 with a phase of another clock signal INTRCLK 60 (see also column 8, lines 12-15). In contrast, claim 9 recites a phase detector and control circuit to compare a phase of a "data signal" and a phase of a "clock signal" on the output clock node. Further, Applicant is unable to find in Leung "phase detector including a clock node to receive the clock signal from the input clock node, and a data node to receive the data signal".

Based on at least the reasons presented above, Applicant submits that claim 9 is not anticipated by Leung. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 9.

Dependent claims 10-12 and 17 depend from claim 9 and recite the things of claim 9. Thus, Applicant believes that claims 10-12 and 17 are also not anticipated by Leung for at least the reasons presented above regarding claim 9, and for the additional things recited in claims 10-12 and 17. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claims 10-12 and 17.

Claims 9-11, 13, and 16 were rejected under 35 USC § 102(e) as being anticipated by Wente et al. (U.S. 6.438.721, hereinafter Wente).

Claim 9 is amended and recites, among other things, a phase detector and control circuit to compare a phase of a "data signal" and a phase of a "clock signal" on the output clock node and to create interpolator control signals, the "phase detector including a clock node to receive the clock signal from the input clock node, and a data node to receive the data signal".

Wente teaches in FIG. 1 a phase detector 12 to compare a phase of a *clock* signal SYNCLK with a phase of *another clock* signal PCLK. In contrast, claim 9 recites a phase detector and control circuit to compare a phase of a "data signal" and a phase of a "clock signal" on the output clock node. Further, Applicant is unable to find in Wente "phase detector including a clock node to receive the clock signal from the input clock node, and a data node to receive the data signal".

Based on at least the reasons presented above, Applicant submits that claim 9 is not anticipated by Wente. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 9.

Dependent claims 10, 11, 13 and 16 depend from claim 9 and recite the things of claim 9. Thus, Applicant believes that claims 10, 11, 13 and 16 are also not anticipated by Wente for at least the reasons presented above regarding claim 9, and for the additional things recited in claims 10, 11, 13 and 16. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claims 10, 11, 13 and 16.

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Serial Number: 09:894.486 Filling Date: June 28, 2001 Title: CLOCK RECOVERY USING CLOCK PHASE INTERPOLATOR

Assignee: Intel Corporation

Allowable Subject Matter

Claims 2-8 and 19-28 were allowed.

Applicant acknowledges the allowance of claims 2-8 and 19-28.

Claims 14-15 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 is rewritten in independent form. The rewriting does not alter the scope of claim 14. Thus, claim 14 and its dependent claim 15 are now in condition for allowance.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Serial Number: 09/894.486

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 20 April 2006

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Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria. VA 22313-1450, on this 20th day of April, 2009.

Mame Horrart

Signatur